UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,183	08/30/2006	Hitoshi Ohmuro	295589US40PCT	7761

22850 7590 07/17/2009

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
RIVAS, SALVADOR E

ART UNIT	PAPER NUMBER
2419	

NOTIFICATION DATE	DELIVERY MODE
07/17/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/591,183	OHMURO ET AL.	
	Examiner	Art Unit	
	SALVADOR E. RIVAS	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 7, 13, and 14* is/are rejected.

7)☒ Claim(s) *2-6 and 8-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/30/2006, 10/26/2007, 4/11/2008, and 4/3/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) and 365(a), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement filed on August 30, 2006 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because on the page 3 of IDS entitled STATEMENT OF RELEVANCY, #2 has been completed left blank and the applicant either needs to complete the STATEMENT OF RELEVANCY page or delete #2 . It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

The information disclosure statements submitted on October 26, 2007, April 11, 2008, and April 3, 2009 have been considered by the Examiner and made of record in the application file.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 13 is rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a particular apparatus), or (2) transform underlying subject matter (such as an article or material) to a different state or thing (Reference the May 15, 2008 memorandum issued by Deputy Commissioner for Patent Examining Policy, John J. Love, titled "Clarification of 'Processes' under 35 U.S.C. 101"). The instant claims neither transform underlying subject matter nor positively tie to another statutory category that accomplishes the claimed method steps, and therefore do not qualify as a statutory process.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Agrawal et al. (U.S. Patent # 5,623,483)**, in view of **Florencio et al. (U.S. Patent Application Publication #2005/0058145 A1)**, and further in view of **Okada et al. (U.S. Patent # 5,809,454)**.

Regarding **claim 1**, Agrawal et al. teach a reproducing method for receiving a stream of sent audio packets (read as data packets) containing an audio code generated by encoding an input audio data stream frame by frame and reproducing an audio signal (read as “synchronization methods and apparatus for synchronizing the delivery of data packets received over such networks.” Column 1 Lines 7-9),

comprising the steps of:

(a) storing received packets in a receiving buffer (read as packet data storage block (Fig.1 @ 260)) (“receiving data packets from the network, storing selected data packets for a selective period of time, …” Column 2 Lines 16-17);

(b) detecting the largest delay jitter (read as Maximum Acceptable Delay (MAD)) and the number of buffered packets ("Control circuit 10 configures and initializes the buffer circuit 20 to receive and process the stream data." Column 2 Lines 53-54),

the largest jitter (read as Maximum Acceptable Delay (MAD)) being any of the largest value and statistical value of jitter (read as Total End-to-End Delay (TED)) obtained by observing arrival jitter of the received packets over a given period of time (read as Packet Delay Distribution (PDD) function; "… PDD data may be developed over time by control circuit 10 …The PDD models are stored at block 15 in FIG. 1 as a look-up table of values or as a function which is periodically evaluated by a suitable processor." (Colum 3 Lines 7-13) Also, "Control circuit 10 calculates a total end-to-end delay value TED for each stream." (Column 3 Lines 20-21) Furthermore, "the minimum value for the TED is limited by the maximum packet loss rate MPLR specified for the stream as a function of the PDD. On the other hand, the maximum value for the TED is limited by the maximum acceptable delay value MAD specified for the stream.

Control circuit 10 thus calculates the operating TED for the stream based upon the MPLR, MAD, and PDD." Column 3 Lines 29-35) and

the number of buffered packets being the number of packets stored in the receiving buffer (Fig.1 @ 260) ("Control circuit 10 calculates a set of buffer configuration parameters for each data stream and allocates buffer resources for each stream, …" Column 3 Lines 15-17);

(c) obtaining, based on the largest delay jitter, an optimum number of buffered packets by using a predetermined relation between the largest

delay jitter and the optimum number of buffered packets ("Control circuit 10 calculates the buffer size requirements for the stream using the packet size S_p, packet rate T_r, and the total end-to-end delay TED." Column 3 Lines 40-42),

the optimum number of buffered packets being the optimum number of packets to be stored in the receiving buffer (Fig.1 @ 260) ("Control circuit 10 allocates a block of memory 260 having S_B bytes and a pointer list 202 having PS slots for buffering each stream." Column 3 Lines 40-42);

(d) determining, on a scale of a plurality of levels, the difference between the detected number of buffered packets and the optimum number of buffered packets.(read as "buffer control circuit 200 may calculate the network delay ND for each packet by subtracting the buffer delay BD from the total end-to-end delay TED. Using the calculated network delays, the PDD model stored in PDD memory may be updated by control circuit 10 to reflect changing network operating characteristics. Control circuit 10 may also update the buffer operating characteristics, i.e., TED, buffer size, and pointer list in response to a changing PDD or PLR." (Column 6 Lines 9-17))

However, Agrawal fail to explicitly teach the method steps comprising:

(e) retrieving a packet corresponding to the current frame from the receiving buffer and decoding an audio code in the packet to obtain a decoded audio data stream in the current frame; and

(f) performing any of expansion, reduction, and preservation of a waveform of the decoded audio data stream in accordance with a rule to make

the number of buffered packets close to the optimum number of buffered packets,

the rule being established for each level of the difference, and outputting the result as audio data of the current frame.

Florencio et al. teach “a system and method for providing automatic jitter control and packet loss concealment for audio signals broadcast across a packet-based network or communications channel.” (Paragraph [0001]) Furthermore, Florencio et al. teach retrieving a packet corresponding to the current frame from the receiving buffer and decoding an audio code in the packet to obtain a decoded audio data stream in the current frame. (read as “the adaptive audio playback controller operates by first using a conventional codec for decoding and reading received packets into a signal buffer as soon as those packets have been received and decoded into signal frames. Samples of the decoded audio signal are then played out of the signal buffer according to the needs of the player device.”(Paragraph [0049]))

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the function for decoding data packets found in a signal buffer as taught by Florencio et al. within the system processing multimedia streams as taught by Agrawal et al. for the purpose of synchronizing data packets.

However, Agrawal et al. and Florencio et al. fail to teach the method steps comprising:

(f) performing any of expansion, reduction, and preservation of a waveform of the decoded audio data stream in accordance with a rule to make

the number of buffered packets close to the optimum number of buffered packets,

the rule being established for each level of the difference, and outputting the result as audio data of the current frame.

Okada et al. teach "...an audio reproducing apparatus capable of reproducing voices that are natural and comfortable to hear, even in a variable speed playback mode." (Column 3 Lines 60-62) Furthermore, Okada et al. teach the method of performing any of expansion, reduction, and preservation of a waveform of the decoded audio data stream (read as voice speed converting unit) in accordance with a rule (read as an index signal) to make the number of buffered packets close to the optimum number of buffered packets (read as "The index adding circuit adds an index signal as information associated with time to the audio signal before the audio signal is stored in a memory of the voice speed converting unit." (Column 4 Lines 38-41)), the rule (read as an index signal) being established for each level of the difference, and outputting the result as audio data of the current frame.("The voice speed converting unit performs voice speed conversion on the audio signal in such a manner that when a bit rate is higher than a normal bit rate, a pitch of a sound interval to be reproduced becomes substantially the same as that in a normal playback mode and a voice speed in the sound interval approaches a voice speed in a sound interval in the normal playback mode. The voice speed converting unit further performs voice speed conversion on the audio signal in such a manner that when the bit rate is lower than the normal bit rate, interruption of the sound interval becomes less noticeable." (Column 4 Lines 9-20))

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the function voice speed conversion as taught by Okada et al. and the function for decoding data packets found in a signal buffer as taught by Florencio et al. within the system processing multimedia streams as taught by Agrawal et al. for the purpose of synchronizing data packets.

Regarding **claim 13**, and **as applied to claim 1 above**, Agrawal et al. (1) teach "synchronization methods and apparatus for synchronizing the delivery of data packets received over such networks." (Column 1 Lines 7-9).

Okada et al. teach "...an audio reproducing apparatus capable of reproducing voices that are natural and comfortable to hear, even in a variable speed playback mode." (Column 3 Lines 60-62)

However, Agrawal et al. and Okada et al. fail to explicitly teach a reproducing program for audio packets written in a computer-interpretable language for causing a computer to perform the reproducing method.

Florencio et al. teach "a system and method for providing automatic jitter control and packet loss concealment for audio signals broadcast across a packet-based network or communications channel." (Paragraph [0001]) Furthermore, Agrawal et al. (2) teach a reproducing program (read as data and/or program modules) for audio packets written in a computer-interpretable language for causing a computer to perform the reproducing method. ("The system memory 130 includes computer storage media in the form of volatile and/or nonvolatile memory such as read only memory (ROM) 131 and random access memory (RAM) 132. ... RAM 132 typically contains data and/or

program modules that are immediately accessible to and/or presently being operated on by processing unit 120."Paragraph [0040])

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the system storage architecture as taught by Florencio et al. with the system processing multimedia streams as taught by Agrawal et al. to store the function for executing voice speed conversion to audio packets as taught by Okada et al. for the purpose of synchronizing data packets.

Regarding **claim 14**, and **as applied to claim 13 above**, Agrawal et al. (1) teach "synchronization methods and apparatus for synchronizing the delivery of data packets received over such networks." (Column 1 Lines 7-9).

Okada et al. teach "...an audio reproducing apparatus capable of reproducing voices that are natural and comfortable to hear, even in a variable speed playback mode." (Column 3 Lines 60-62)

However, Agrawal et al. (1) and Okada et al. fail to explicitly teach a computer-readable recording medium and having recorded thereon the reproducing program.

Florencio et al. teach "a system and method for providing automatic jitter control and packet loss concealment for audio signals broadcast across a packet-based network or communications channel." (Paragraph [0001]) Furthermore, Florencio et al. (2) teach a computer-readable recording medium (read as system memory (Fig,1 @ 130)) and having recorded thereon the reproducing program (read as data and/or program modules). ("The system memory 130 includes computer storage media in the form of volatile and/or nonvolatile memory such as read only memory (ROM) 131 and

random access memory (RAM) 132. … RAM 132 typically contains data and/or program modules that are immediately accessible to and/or presently being operated on by processing unit 120."Paragraph [0040])

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the function voice speed conversion as taught by Okada et al. and the function for decoding data packets found in a signal buffer as taught by Florencio et al. within the system processing multimedia streams as taught by Agrawal et al. for the purpose of synchronizing data packets.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the system storage architecture as taught by Florencio et al. with the system processing multimedia streams as taught by Agrawal et al. to store the function for executing voice speed conversion to audio packets as taught by Okada et al. for the purpose of synchronizing data packets.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Okada et al. (U.S. Patent # 5,809,454)**, in view of **Agrawal et al. (U.S. Patent # 5,623,483)**, and further in view of **Florencio et al. (U.S. Patent Application Publication #2005/0058145 A1)**.

Regarding **claim 7**, Okada et al. teach a reproducing apparatus (Fig.1 @ 4) for audio packets which receives a stream of sent audio packets containing an audio code generated by encoding an input audio data stream frame by frame and reproduces an audio signal (read as "an MPEG audio reproducing apparatus having a voice speed

converting function and to an MPEG video/audio reproducing apparatus having the MPEG audio reproducing apparatus and a video decoder." Column 1 Lines 10-13),

comprising:

a packet receiving part (Fig.1 @ 13) which receives audio packets from a packet communication network;

a receiving buffer (Fig.1 @ 34) for temporarily storing the received packets and reading out packets in response to a request;

generates a control signal (read as index adding circuit) for instructing to perform any of expansion, reduction, and preservation of a waveform of the decoded audio data stream in accordance with a rule (read as index signal) to make the number of buffered packets close to the optimum number of buffered packets, the rule (read as index signal) being established for each level of the difference (read as "The index adding circuit adds an index signal as information associated with time to the audio signal before the audio signal is stored in a memory of the voice speed converting unit." (Column 4 Lines 38-41));

a consumption adjusting part (read as a voice converting circuit) which performs any of expansion, reduction, and preservation of the waveform of the decoded audio data stream in accordance with the control signal and outputs the result as sound data of the current frame. ("The voice speed converting unit performs voice speed conversion on the audio signal in such a manner that when a bit rate is higher than a normal bit rate, a pitch of a sound interval to be reproduced becomes substantially the same as that in a normal playback mode and a voice speed in the sound interval

approaches a voice speed in a sound interval in the normal playback mode. The voice speed converting unit further performs voice speed conversion on the audio signal in such a manner that when the bit rate is lower than the normal bit rate, interruption of the sound interval becomes less noticeable." (Column 4 Lines 9-20))

However, Okada et al. fail to teach a state detecting part which detects the largest delay jitter and the number of buffered packets,

the largest jitter being any of the largest value and statistical value of jitter obtained by observing arrival jitter of the received packets over a given period of time and

the number of buffered packets being the number of packets stored in the receiving buffer;

a control part which obtains based on the largest delay jitter an optimum number of buffered packets by using a predetermined relation between the largest delay jitter and the optimum number of buffered packets,

the optimum number of buffered packets being the optimum number of packets to be stored in the receiving buffer,

determines, on a scale of a plurality of levels, the difference between the detected number of buffered packets and the optimum number of buffered packets, and

an audio packet decoding part which decodes an audio code in a packet corresponding to the current frame extracted from the receiving buffer to obtain a decoded audio data stream in the current frame.

Agrawal et al. teach "synchronization methods and apparatus for synchronizing the delivery of data packets received over such networks." (Column 1 Lines 7-9) Furthermore, Agrawal et al. teach a state detecting part (Fig.1 @ 10) which detects the largest delay jitter (read as Maximum Acceptable Delay (MAD)) and the number of buffered packets, ("Control circuit 10 configures and initializes the buffer circuit 20 to receive and process the stream data." Column 2 Lines 53-54),

the largest jitter (read as Maximum Acceptable Delay (MAD)) being any of the largest value and statistical value of jitter (read as Total End-to-End Delay (TED)) obtained by observing arrival jitter of the received packets over a given period of time (read as Packet Delay Distribution (PDD) function; "… PDD data may be developed over time by control circuit 10 …The PDD models are stored at block 15 in FIG. 1 as a look-up table of values or as a function which is periodically evaluated by a suitable processor." (Colum 3 Lines 7-13) Also, "Control circuit 10 calculates a total end-to-end delay value TED for each stream." (Column 3 Lines 20-21) Furthermore, "the minimum value for the TED is limited by the maximum packet loss rate MPLR specified for the stream as a function of the PDD. On the other hand, the maximum value for the TED is limited by the maximum acceptable delay value MAD specified for the stream.

Control circuit 10 thus calculates the operating TED for the stream based upon the MPLR, MAD, and PDD." Column 3 Lines 29-35) and

the number of buffered packets being the number of packets stored in the receiving buffer (Fig.1 @ 260) ("Control circuit 10 calculates a set of buffer configuration

parameters for each data stream and allocates buffer resources for each stream, …" Column 3 Lines 15-17);

a control part (Fig.1 @ 10) obtaining, based on the largest delay jitter an optimum number of buffered packets by using a predetermined relation between the largest delay jitter and the optimum number of buffered packets ("Control circuit 10 calculates the buffer size requirements for the stream using the packet size S_p, packet rate T_r, and the total end-to-end delay TED." Column 3 Lines 40-42),

the optimum number of buffered packets being the optimum number of packets to be stored in the receiving buffer (Fig.1 @ 260) ("Control circuit 10 allocates a block of memory 260 having S_B bytes and a pointer list 202 having PS slots for buffering each stream." Column 3 Lines 40-42);

determining, on a scale of a plurality of levels, the difference between the detected number of buffered packets and the optimum number of buffered packets. (read as "buffer control circuit 200 may calculate the network delay ND for each packet by subtracting the buffer delay BD from the total end-to-end delay TED. Using the calculated network delays, the PDD model stored in PDD memory may be updated by control circuit 10 to reflect changing network operating characteristics. Control circuit 10 may also update the buffer operating characteristics, i.e., TED, buffer size, and pointer list in response to a changing PDD or PLR." (Column 6 Lines 9-17))

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the configuration control circuit as taught by Agrawal et al. within the audio reproducing system as taught by Okada et al. for the

purpose of synchronizing audio packets to be able to satisfy a wide range of application and user requirements.

However, Okada et al. and Agrawal et al. fail to teach an audio packet decoding part which decodes an audio code in a packet corresponding to the current frame extracted from the receiving buffer to obtain a decoded audio data stream in the current frame.

Florencio et al. teach “a system and method for providing automatic jitter control and packet loss concealment for audio signals broadcast across a packet-based network or communications channel.” (Paragraph [0001]) Furthermore, Florencio et al. teach an audio packet decoding part (read as CODEC module (Fig.2 @ 220)) which decodes an audio code in a packet corresponding to the current frame extracted from the receiving buffer to obtain a decoded audio data stream in the current frame. (read as “the adaptive audio playback controller operates by first using a conventional codec for decoding and reading received packets into a signal buffer as soon as those packets have been received and decoded into signal frames. Samples of the decoded audio signal are then played out of the signal buffer according to the needs of the player device.”(Paragraph [0049]))

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the function for decoding data packets found in a signal buffer as taught by Florencio et al. and the configuration control circuit as taught by Agrawal et al. within the audio reproducing system as taught by Okada et al.

for the purpose of synchronizing audio packets to be able to satisfy a wide range of application and user requirements.

Allowable Subject Matter

5. **Claims 2-6 and 8-12** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: **Agrawal et al.(2) (U.S. Patent # 6,072,809)**.

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or early communications from the Examiner should be directed to Salvador E. Rivas whose telephone number is (571) 270-1784. The examiner can normally be reached on Monday-Friday from 7:00AM to 3:30PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Chirag G. Shah can be reached on (571) 272- 3144. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Salvador E. Rivas
S.E.R./ser

July 10, 2009

/Gregory B Sefcheck/

Primary Examiner, Art Unit 2419